HAW Kiel
Hochschule für Angewandte Wissenschaften Kiel
Kiel University of Applied Sciences

BK107 - ASIC-Design / VHDL

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General information	
Module Code	BK107
Unique Identifier	
Module Leader(s)	Prof. Dr. Jetzek, Ulrich (ulrich.jetzek@haw-kiel.de)
Lecturer(s)	Prof. Dr. Jetzek, Ulrich (ulrich.jetzek@haw-kiel.de) Rohrandt, Christian (christian.rohrandt@haw-kiel.de)
Offered in Semester	Sommersemester 2019
Module duration	1 Semester
Occurrence frequency	Regular
Module occurrence	In der Regel im Sommersemester
Language	Englisch
Recommended for international students	Yes
Can be attended with different study programme	No

Curricular relevance (according to examination regulations)
Study Subject: B.Eng. - E - Elektrotechnik (PO 2017, V3) Study Specialization: Technische Informatik Module type: Wahlmodul Semester: 4, 5, 6, 7
Study Subject: B.Eng. - E - Elektrotechnik (PO 2017, V3) Study Specialization: Kommunikationstechnik und Embedded Systems Module type: Wahlmodul Semester: 5, 6
Study Subject: B.Eng. - Me (PO 2023) - Mechatronik (PO 2023, V4) Module type: Wahlmodul Semester: 4, 5, 6
Study Subject: B.Eng. - Wing - Wirtschaftsingenieurwesen - Elektrotechnik (PO 2017, V1) Study Specialization: Kommunikationstechnik Module type: Wahlmodul Semester: 5, 6
Study Subject: B.Eng. - Wing - Wirtschaftsingenieurwesen - Elektrotechnik (PO 2017, V1) Study Specialization: Digitale Wirtschaft Module type: Wahlmodul Semester: 4, 5, 6, 7
Study Subject: B.Sc. - INI - Informationstechnologie (PO 2017, V1) Study Specialization: Medieninformatik Module type: Wahlmodul Semester: 4, 5
Study Subject: B.Sc. - INI - Informationstechnologie (PO 2017, V1) Study Specialization: Angewandte Informatik Module type: Wahlmodul Semester: 4, 5

Qualification outcome
Areas of Competence: Knowledge and Understanding; Use, application and generation of knowledge; Communication and cooperation; Scientific self-understanding / professionalism.

Students have understood the concept, syntax and semantics of the Hardware description language VHDL.
Students will apply their VHDL-Knowledge to specific lab-Problems, where they will work with suitable development boards. Students will implement VHDL-designs based on given problems onto the development-baords/FPGAs. Within this module development boards equipped with Xilinx FPGAs will be used.
Students will work in small tams in the lab Environment and will learn to solve problems in a team.
Within this module students will learn: - how to analyze a specific digital circuit Problem - how to design VHDL-Code in order to solve digital circuit Problems - how to simulate their VHDL-Code - how to synthesize their VHDL Code and to program an FPGA - how to test and verify their VHDL-Code on an FPGA/development board

Content information	
Content	- synthesis of simple combinatorial logic in VHDL - desgin of digital functions and function elements in VHDL using processes - modelling of tri-state-elements and don't care states in VHDL - design of finite state machines and synchronous counters in VHDL - structured VHDL designs using main and sub modules
Literature	- Jürgen Reichardt, Bernd Schwarz: „VHDL Synthese – Entwurf digitaler Schaltungen und Systeme“, Oldenbourg Verl., 5.Aufl., 2009 - Pong P. Chu: “FPGA Prototyping by VHDL-Examples”, Wiley & Sons, 2008

Teaching formats of the courses	
Teaching format	**SWS**
Lehrvortrag	2
Labor	2

Workload	
Number of SWS	4 SWS
Credits	5,00 Credits
Contact hours	48 Hours
Self study	102 Hours

Module Examination	
Examination prerequisites according to exam regulations	None
BK107 - Übung	Method of Examination: Übung Weighting: 0% wird angerechnet gem. § 11 Absatz 2 PVO: Yes Graded: No
BK107 - Klausur	Method of Examination: Klausur Duration: 90 Minutes Weighting: 100% wird angerechnet gem. § 11 Absatz 2 PVO: Yes Graded: Yes

Miscellaneous	
Miscellaneous	Alle Laborberichte müssen durch Testat anerkannt sein. Nur dann gilt das Labor als bestanden.