HAW Kiel
Hochschule für Angewandte Wissenschaften Kiel
Kiel University of Applied Sciences

MK114 - FPGA Prototyping by VHDL examples

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General information	
Module Code	MK114
Unique Identifier	
Module Leader(s)	Prof. Dr. Jetzek, Ulrich (ulrich.jetzek@haw-kiel.de)
Lecturer(s)	Prof. Dr. Jetzek, Ulrich (ulrich.jetzek@haw-kiel.de) Rohrandt, Christian (christian.rohrandt@haw-kiel.de)
Offered in Semester	Sommersemester 2019
Module duration	1 Semester
Occurrence frequency	Regular
Module occurrence	In der Regel im Sommersemester
Language	Englisch
Recommended for international students	Yes
Can be attended with different study programme	No

Curricular relevance (according to examination regulations)
Study Subject: M.Eng. - MET - Elektrische Technologien (PO 2017, V3) Study Specialization: Kommunikationstechnik und Embedded Systems Module type: Wahlmodul Semester: 1, 2
Study Subject: M.Eng. - MET - Elektrische Technologien (PO 2017, V3) Study Specialization: Elektrische Energietechnik Module type: Wahlmodul Semester: 1, 2
Study Subject: M.Eng. - MET - Elektrische Technologien (PO 2017, V3) Study Specialization: Mechatronik Module type: Wahlmodul Semester: 1, 2
Study Subject: M.Sc. - MIE - Information Engineering (PO 2022, V3) Study Specialization: IT Security Module type: Wahlmodul Semester: 1, 2, 3
Study Subject: M.Sc. - MIE - Information Engineering (PO 2022, V3) Study Specialization: Information Technology and Systems Module type: Wahlmodul Semester: 1, 2, 3
Study Subject: M.Sc. - MIE - Information Engineering (PO 2022, V3) Study Specialization: Intelligent Systems Module type: Wahlmodul Semester: 1, 2, 3

Qualification outcome
Areas of Competence: Knowledge and Understanding; Use, application and generation of knowledge; Communication and cooperation; Scientific self-understanding / professionalism.

The students have understood the fundamentals of the Hardware Description Language VHDL. They know the principle how to design combinatorial as well as sequential circuits and how to implement a finite state machine in VHDL. They are able to apply this knowledge to design regular sequential circuits like Counters or shift Registers as well as circuits for finite state machines. The students know how to partition a System into control and data plane and how to implement the corresponding circuits in VHDL.They know how to set up a testbench and are capable of simulating VHDL designs as well as how to set up simple testing circuits to a specific VHDL design on a development board.
Within the lab exercises, the students have the possibility to apply their knowledge by implementing given problems on a development board and to validate their implementation approach.
The students work together in small teams in the lab. Therefore they are capable of structuring lab exercises into different work packages, to discuss and solve problems, which occur throughout the implementation process, within the team and they are able to document their lab exercise results in a systematic and structured way.

Content information	
Content	- synthesis of combinational digital circuits - structured VHDL coding - design of digital functions using the VHDL concept of ‚processes' - design and verification of sequential circuits - design and verification of finite state machines - control and usage of common technical components like UART, FIFO or VGA (graphics). The different topics will be implemented on the ZED-Board, which is a powerful Xilinx development board equipped with a Zynq System-on-Chip (SoC).
Literature	- Jürgen Reichardt, Bernd Schwarz: „VHDL Synthese – Entwurf digitaler Schaltungen und Systeme", Oldenbourg Verl., 5.Aufl., 2009 - Pong P. Chu: "FPGA Prototyping by VHDL-Examples", Wiley & Sons, 2008

Teaching formats of the courses	
Teaching format	**SWS**
Labor	2
Lehrvortrag	2

Workload	
Number of SWS	4 SWS
Credits	5,00 Credits
Contact hours	48 Hours
Self study	102 Hours

Module Examination	
Examination prerequisites according to exam regulations	None
MK114 - Übung	Method of Examination: Übung Weighting: 0% wird angerechnet gem. § 11 Absatz 2 PVO: Yes Graded: No
MK114 - Klausur	Method of Examination: Klausur Duration: 90 Minutes Weighting: 100% wird angerechnet gem. § 11 Absatz 2 PVO: Yes Graded: Yes